6549235

1/10

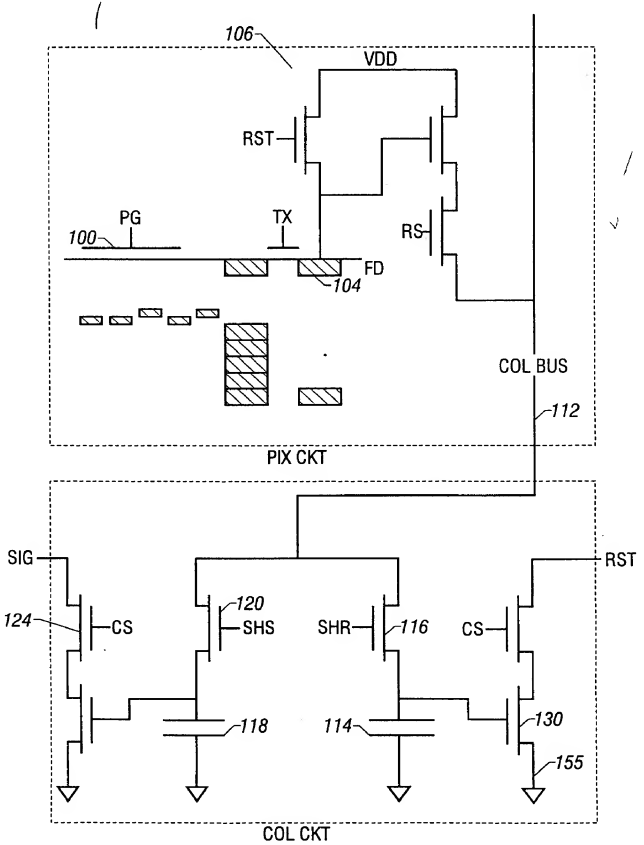


FIG. 1

09.02

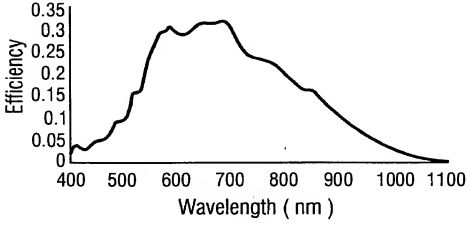


FIG. 2

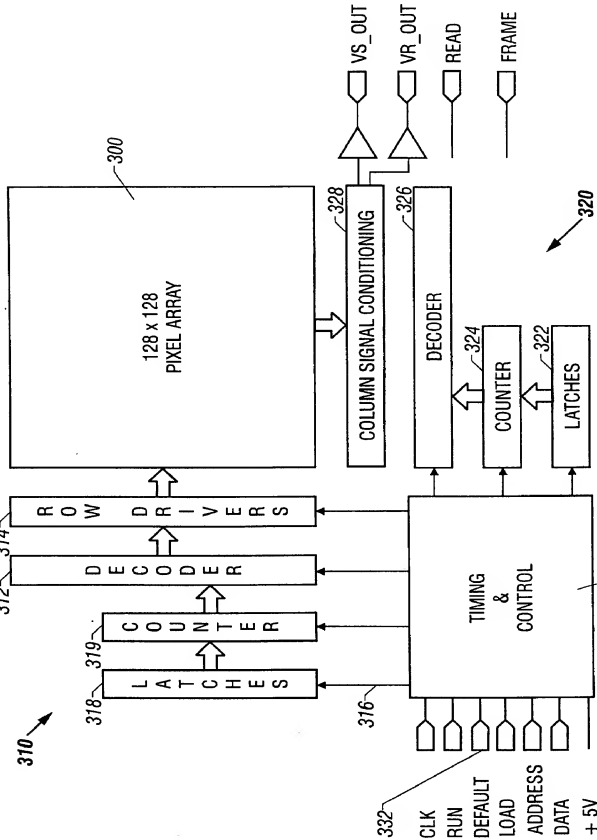


FIG. 3

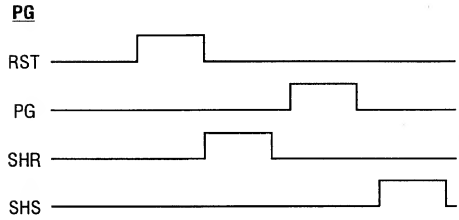


FIG. 4A

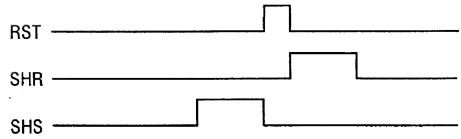


FIG. 4B

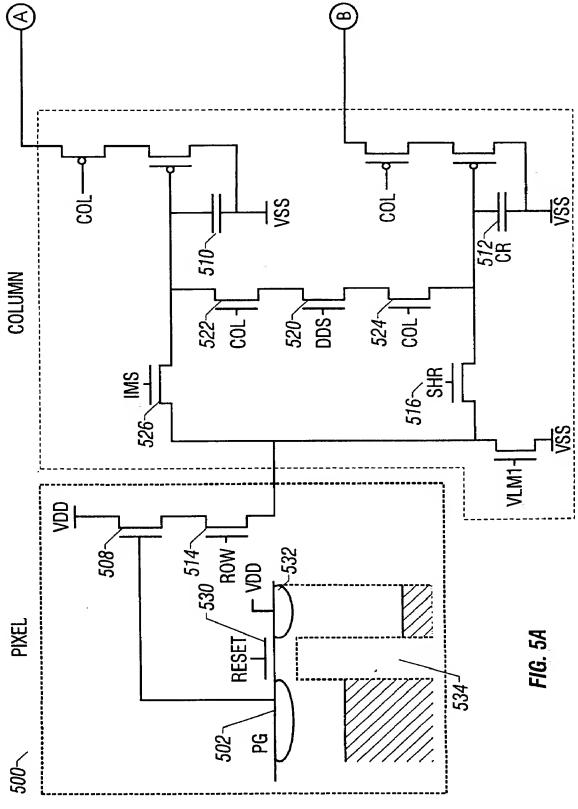


FIG. 5A

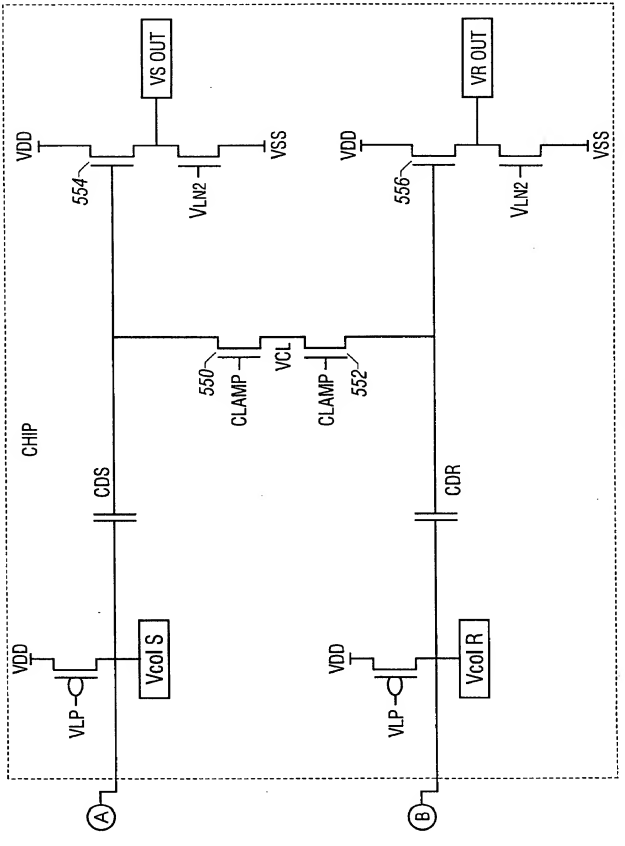


FIG. 5B

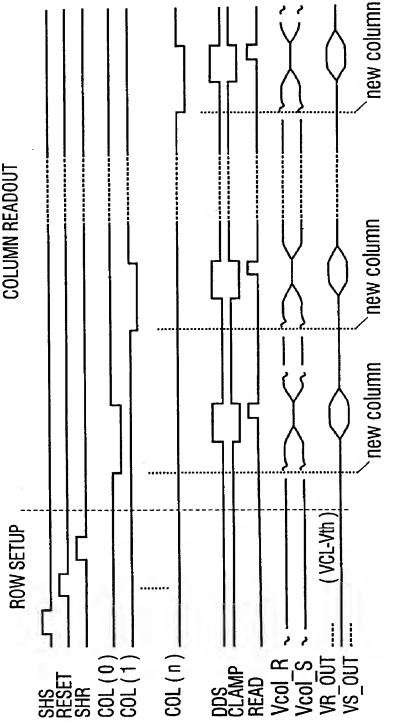


FIG. 6

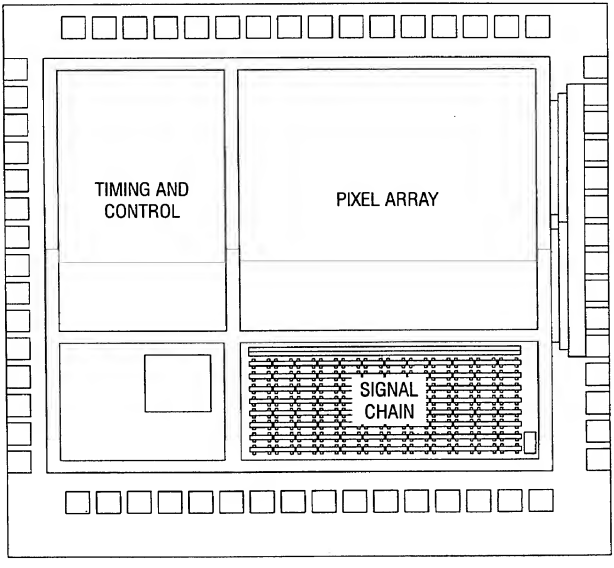


FIG. 7

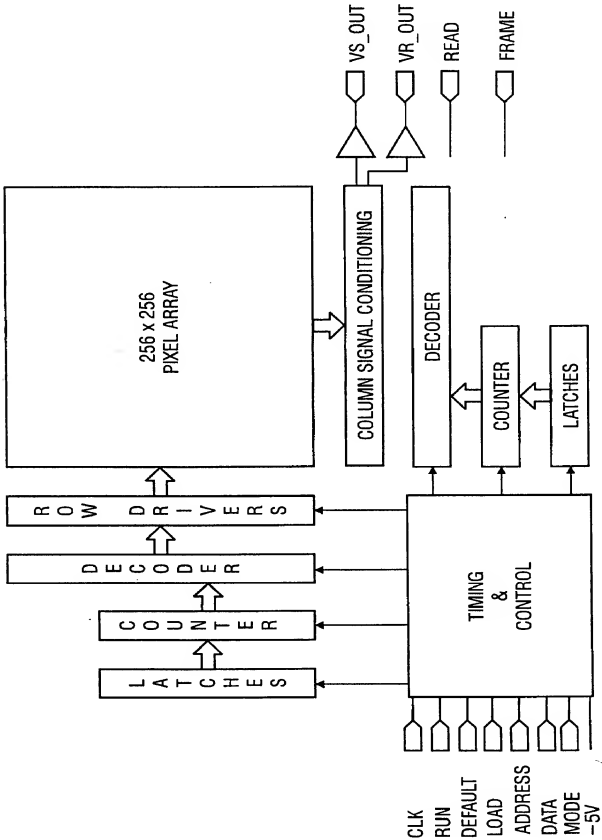
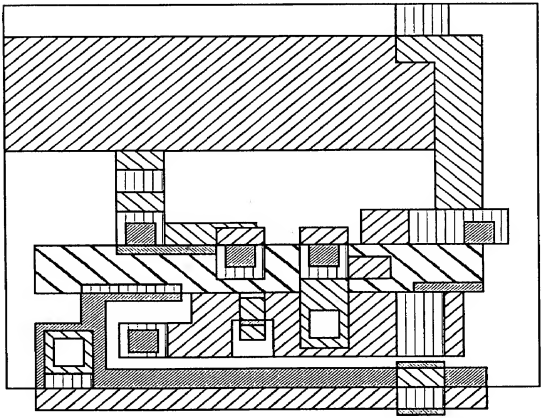


FIG. 8



Array Size	256 x 256
Pixel Size	20.4 μm
Technology	1.2 μm n-well CMOS (HP)
Maximum Clock Rate	10 MHz
Minimum Clock Rate	none
Maximum Pixel Rate	2.5 MHz
Maximum Integration Delay	16 x 10^9 clock periods or 1600 secs at 10 MHz

FIG. 9